AMENDMENTS TO THE SPECIFICATION:

Please amend Paragraph [0019] of the published application as follows:

[0019] FIG. 1 illustrates in block diagram form a transceiver according to the invention comprising a single direct digital synthesizer driven phase locked loop (DDS driven PLL) 24,10-15 according to the invention having a direct digital synthesizer (DDS) 24 according to the invention and a phase locked loop (PLL) 10-15 according to the invention. The transceiver comprises an antenna 1 coupled to an in/output of a switch 3 of which an input is coupled to an output of a ~~transceiver~~ transmitter part 2 and of which an output is coupled to an input of a receiver part 4. An input of transmitter part 2 is coupled to a first output of a switch 5, of which a second output is coupled to a first input of a demodulator 6 and of which an input is coupled to an output of PLL 10-15. A second input of demodulator 6 is coupled to an output of receiver part 4 and an output of demodulator 6 is coupled to an input of a controller 40.